REMARKS

Claims 1-12 are presented for examination. Claims 4, 11 and 12 have been cancelled without prejudice or disclaimer. Claims 1, 7 and 9 have been amended.

FIG 1 has been corrected per the Examiner's request to label the second data line as GIO1, instead of GIO10.

The specification has been amended per the Examiner's request to delete "the" before "two EXOR circuits" on page 10. Also, the disclosure on page 6 has been corrected to replace "GIOa-GIOn" with --GIO0-GIOn--.

Claims 7 and 9 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. In response, these claims have been corrected to clarify their language.

In particular, claim 7, as amended, clarifies that the teacher data bit is represented by a data bit located in a corresponding position in a different group from a corresponding group including the corresponding data.

Claim 9, as amended, recites that each of the data bits is received by the same number of the first determining circuits.

Claims 1-4, 6-9, and 11-12 have been rejected under 35 U.S.C. § 102(b) as being anticipated by McClure et al. Dependent claim 5 has been rejected under 35 U.S.C. § 103 as being unpatentable over McClure et al. in view of Uchida. Dependent claim 10 has been rejected under 35 U.S.C. § 103 as being unpatentable over McClure et al. in view of Tomishima et al.

Claim 1 recites a multi-bit test circuit for determining a match in logical level among a plurality of data bits read out in parallel from a memory array. The test circuit comprises:

a plurality of first determining circuits, arranged corresponding to said plurality of data bits, each for receiving, as a pair, a corresponding data bit and a teacher data bit placed in a predetermined relation with said corresponding data bit in the plurality of data bits, and determining a match in logical level between received data bits, data bits in each pair including different teacher data bits from other pair(s); and

a final determining circuit for outputting a final determination signal indicating a match in logical level among said plurality of data bits in accordance with output signals of said plurality of first determining circuits.

To more clearly define the claimed invention over the reference, claim 1 has been amended to recite that the plurality of data bits is divided into at least three groups, and the first determining circuits are arranged such that a data bit in a group of said at least three groups is compared with a data bit in each of other two groups. The claim specifies that the number of the plurality of first determining circuits is the same as the number of the plurality of data bits.

The Examiner considers comparators 500 and 501 (FIG. 3 of McClure et al.) to correspond to the claimed first determining circuits, and NAND 58 and inverter 59 to correspond to the claimed final determining circuit.

Considering the reference, McClure discloses a multi-bit test circuit, in which 64 bit data are divided into groups of 8 bit data and adjacent groups of 8 bit data are compared on bit-by-bit basis. In the arrangement of Figs. 3 and 4, the comparators 500 and 501, each including 8 EXNOR gates, compare the set of the data bits 180 and 181 and the set of data bits 182 and 183, respectively. In addition, the comparator 54L includes 8 EXOR gates for

comparing the set of the data bits 181 and 182. Therefore, McClure requires 24 EXOR gates for comparing 32 bit data of four groups 180-183.

The reference does not disclose that the plurality of data bits is divided into at least three groups, and the first determining circuits are arranged such that a data bit in one of the three groups is compared with a data bit in each of other two groups.

In accordance with the claimed arrangement, as shown, for example, in Figs. 3 to 5, the number of the first determining circuits is the same as the number of the data bits. Specifically, 32 bit data may be compared using 32 EXOR gates. As disclosed in the specification on page 10, lines 13-23, in such an arrangement, the output signal of each EXOR gate can be made definite at the same timing. As a result, there is no need to determine the timing of taking in flag FLAG from the OR gate based on the variations in signal propagation delay time because the timing margin can be made large. As a result, a next stage circuit is enabled to take in flag FLAG from the OR gate faster.

As discussed above, in the arrangement of McClure, the number of the EXOR gates is smaller than the number of data bits to be tested, and the signal propagation delay at the gates becomes large, particularly, due to a two-stage comparator arrangement.

Hence, McClure does not show the claimed arrangement allowing the signal propagation delay at the gates to be reduced.

Claims 2, 3 and 5-10 are defined over the prior art at least for the reasons presented above in connection with claim 1.

In view of the foregoing, and in summary, claims 1-3 and 5-10 are considered to be in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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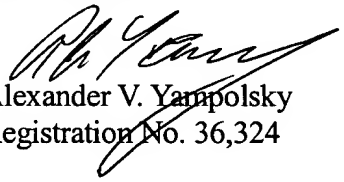

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